Virtex-II Pro PowerPC SEE Characterization Test Methods and Results

Session L: Birds of a Feather

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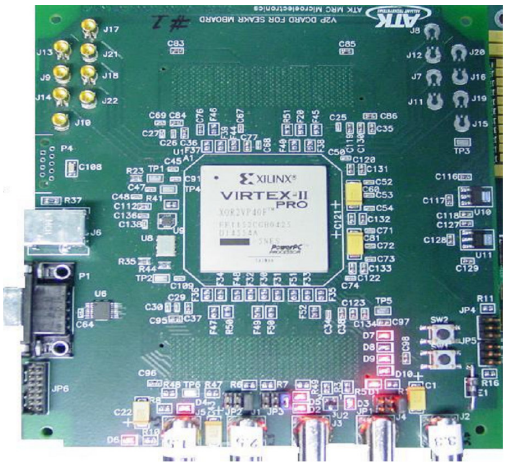
Introduction

- Prior Xilinx Virtex-II Pro SEE testing
  - Memec COTS board
  - Heavy ions at TAMU and MSU
  - Focus: PowerPC, MGTs, and SEL
- Current Xilinx Virtex-II Pro SEE testing
  - Xilinx Radiation Test Consortium board
  - Protons at IUCF
  - Focus: PowerPC(s)

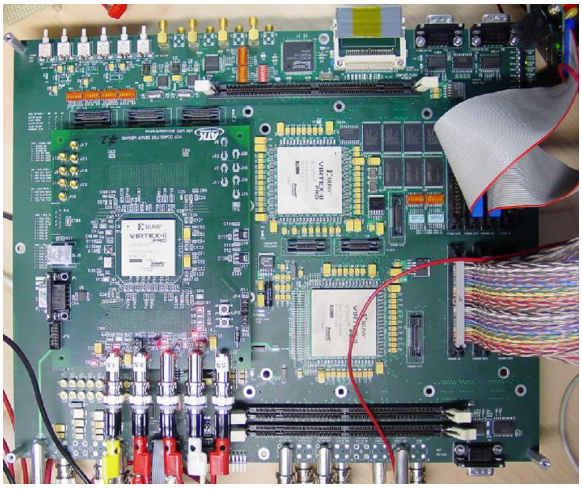
XRTC Board – Daughter Card

- Xilinx Virtex-II Pro
  - XQR2VP40-FF1152
  - Dual PowerPCs
  - 15,868,256 configuration bits
- External interfaces
  - Platform flash devices
  - JTAG/SelectMAP
  - CPU debug headers
  - RS-232
  - 2 300-pin Teradyne connectors
  - SMPX MGTs
- Isolated power lugs
- Available with socket



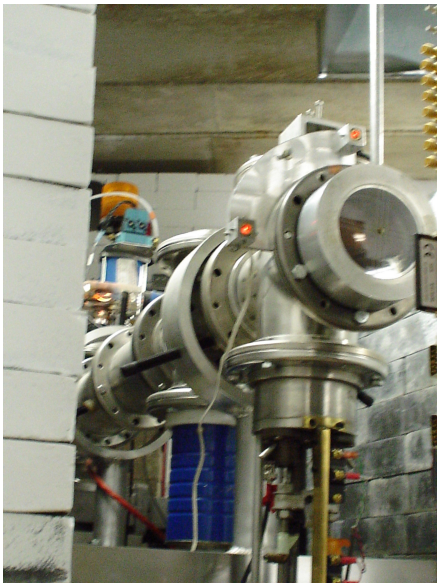
XRTC Board - Motherboard

- 2 XC2VP70 FPGAs
  - DUT configuration scrubber
  - DUT functionality monitor
- External interfaces
  - Platform flash devices
  - System ACE
  - Triple majority voted flash
  - 7 40-pin IDE connectors
  - 3 512-MB SDRAM DIMMs
  - 3 RS-232 ports
  - JTAG/Debug headers
  - MGT clock synthesizer
  - SMPX MGTs

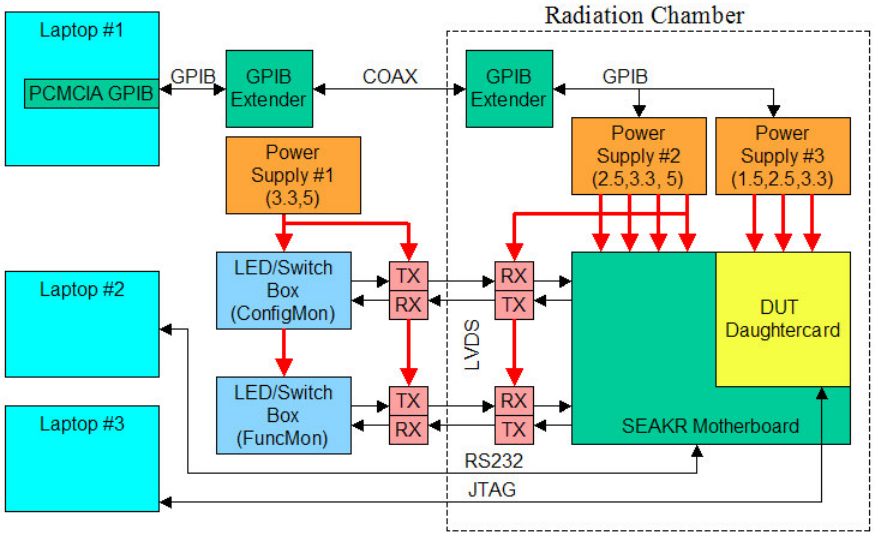


IUCF Test Facility

- Indiana University Cyclotron Facility
  - Bloomington, IN
  - Proton beam
    - Energy: 30 - 200 MeV
    - Flux: 1e2 – 1e11 p/sec-cm^2
  - Cable length distance to user area is 60-70 ft.

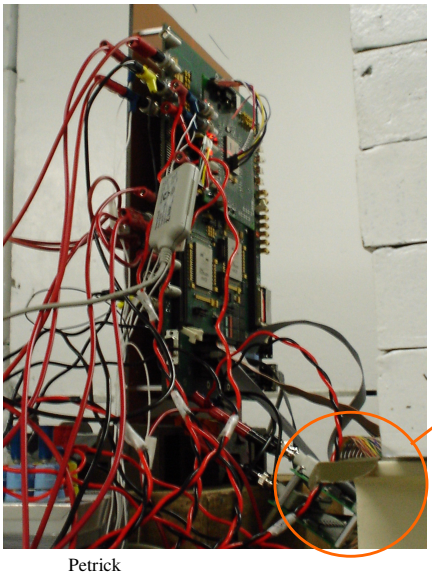


Test Setup

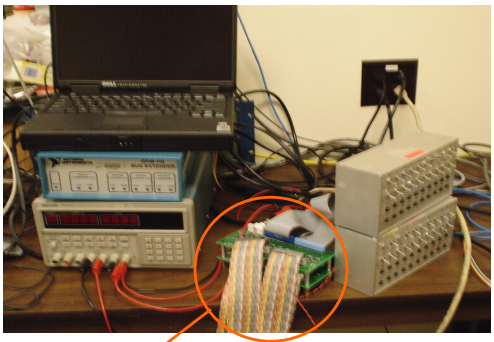


Test Setup Pictures

XRTC Board in Beam

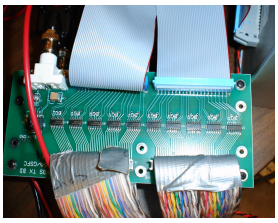


User Area



LVDS Link

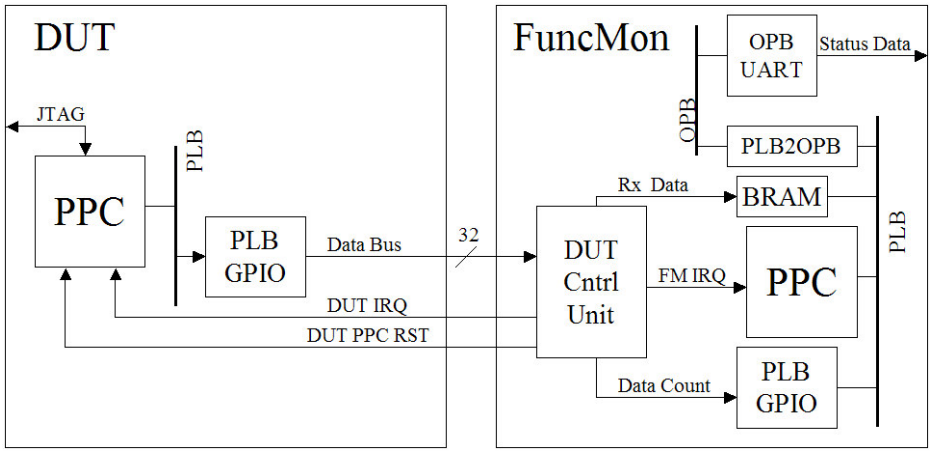
LVDS Transceiver Cards



Test Applications

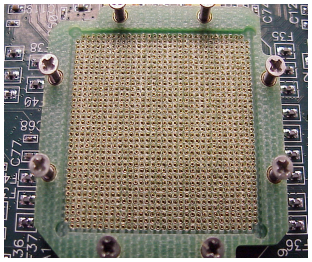
1. Static Register/Cache Test
   - PowerPC initializes registers before each run
   - XMD used to initialize data cache before run, read out register and data cache after run via JTAG
2. "Pseudo-Static" Register Test
   - FuncMon issues IRQs to DUT PowerPC at 1-Hz
   - DUT PowerPC ISR dumps all 80 register values to FuncMon via 32-bit GPIO data bus
   - FuncMon buffers all data received, issues IRQ to its own PowerPC, which dumps data out UART
   - FuncMon also counts reset events and timeout events

Test Application Diagram



Test Complications

- Functionality not integrated for this test
  1. Configuration scrubbing
  2. Design triplication
  3. DUT PowerPC exception handlers
- Connection failures with socketed DUT card
  - 1152-pin spring loaded socket
  - Damaged springs resulted in signal connections including JTAG
  - Static register/cache test was not possible with socketed card



SEE Results

Static Test Bit-Error Results

PowerPC Unit	Total Bit-Errors	Cross (cm^2)	StDev	Cross/bit (cm^2)	StDev
GPRs	4	4.99E-11	2.50E-11	4.88E-14	2.44E-14
D-Cache	87	4.34E-9	2.33E-10	3.31E-14	1.78E-15

Pseudo-Static Test SEE Results

(Note: Each run was stopped when the DUT stopped responding to IRQs)

Computation Method	Cross (cm^2)	StDev
Average of 24 runs	9.54E-10	7.51E-10

- Other observed effects:
  - Processor resets, DUT power cycling required, instruction jumps, program exceptions, irregular response to IRQs, bit-flips in SPRs

Discussion of Results

- Static Test
  - Valid SEU data collected on register and cache
  - For statistical purposes, more testing is required
  - Scrubbing will keep JTAG routing valid, decreasing the number of "bad" runs
- Pseudo-Static Test
  - The runs were not long enough to gather SEU data on the registers
  - Four runs failed during a DUT PowerPC ISR, ***however***:
  - No scrubbing → all runs most likely failed due to configuration upsets rather than a PowerPC SEE
  - Scrubbing and exception handlers will allow SEU data to be collected using this IRQ design scheme

Future Work Plan

- Integrate configuration scrubbing, exception handlers, and TMR into designs
- Add more functionality to test applications
  - Use of dual PowerPCs for data collection
  - Ability to monitor/count program exception types
- Advanced test applications
  - Exercise PowerPC with dynamic test
  - Preliminary PowerPC mitigation test
- Next test date: October 17-19 @ IUCF